REMARKS

Claims 1-4, 7-10, 13-17 and 20-21 are currently pending.

Claims 1-4, 7-10, 13-17 and 20-21 have been rejected.

Claims 22-42 have been previously withdrawn.

Claim 1 has been amended.

Reconsideration of Claims 1-4, 7-10, 13-17 and 20-21 is respectfully requested.

I. CLAIM REJECTIONS -- 35 U.S.C. § 102

Claims 1-3, 7-9, 13-17 and 21 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,902,640 to Sachitano et al. (hereinafter "Sachitano"). In response, the Applicants have amended Claim 1.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 4, October 2005) (*citing In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

The limitations in amended Claim 1 are not taught or suggested in the Sachitano reference. In particular, Sachitano does not teach or suggest that a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain

substantially identical dopant concentrations, as required by amended Claim 1.

The Applicants respectfully submit that the Sachitano reference appears to suggest differentiated doping during formation. (Column 4, Line 55 to Column 5, Line 7; Column 10, Lines 31-51).

For reference purposes, the Applicants set forth below an outline of certain major steps in the manufacture of the Applicants' invention.

A. Paragraph [00112] describes how the Poly 1 layer (2700) is doped to form an extrinsic base in the PNP device and an NMOS gate in the NMOS device.

B. Paragraph [00114] describes how the Poly 1 layer (2700) is doped to form an extrinsic base in the NPN device and a PMOS gate in the PMOS device.

C. Paragraph [00129] describes how the intrinsic base (3410) in the NPN device is doped and how the lightly doped drains (LDD) (3420, 3430) in the PMOS device are doped.

D. Paragraph [00132] describes how the intrinsic base (3510) in the PNP device is doped and how the lightly doped drains (LDD) (3520, 3530) in the NMOS device are doped.

E. Paragraph [00138] describes how the Poly 2 layer (3800) is doped to form (1) NPN emitter 3910 in the NPN device, and (2) NPN deep collector 3920 in the NPN device, and (3) NMOS source/drain 3930 in the NMOS device, and (4) PMOS well contact 3940 in the PMOS device.

F. Paragraph [00141] describes how the Poly 2 layer (3800) is doped to form (1) PNP emitter 4010 in the PNP device, and (2) PNP deep collector 4020 in the PNP device, and (3) NMOS well contact 4030 in the NMOS device, and (4) PMOS source/drain 4040

in the PMOS device.

Now consider the structure and method disclosed in the Sachitano reference.

Before the first polysilicon layer 134 is deposited in Step 29, there is a first implant step (Step 25) that is carried out for the "gate threshold voltages" of the MOS devices. Then there are two implant steps (Steps 26 and 27) that are performed "to implant collector contact region 130 to an increased N+ concentration" in the NPN device (Sachitano, Column 8, Lines 6-12). It is noted that Step 25, Step 26 and Step 27 are performed sequentially. Then the polysilicon layer 134 is deposited. (Step 29) (Sachitano, Column 8, Lines 17-19).

Sachitano then states "This layer [first polysilicon layer 134] is then masked and implanted, first, to implant the polysilicon layer to N+ concentrations over the PMOS and NMOS active device regions and over the collector contact region 130 (steps 30 and 31)." (Sachitano, Column 8, Lines 19-22). This first implant step includes the "gate" portions of the PMOS and NMOS devices. (See Figure 4 of Sachitano).

Then the N+ implant mask is stripped and the substrate is again masked and the first polysilicon layer 134 is "implanted to dope the polysilicon layer overlying the NPN bipolar active region to P+ concentrations (steps 32 and 33)." (Sachitano, Column 8, Lines 23-26). This second implant step includes the "base" portions of the NPN device. (See Figure 4 of Sachitano).

The PMOS and NMOS active device regions of the Sachitano device are implanted to N+ concentrations using an N type dopant (e.g., arsenic, antimony, phosphorus). Table 1 in Column 12 of Sachitano describes the use of phosphorus as the N type dopant. The bipolar NPN device region of the Sachitano device is implanted to P+ concentrations using a P type

dopant (e.g., boron, indium, gallium, aluminum). Table 1 in Column 12 of Sachitano describes the use of boron as the P type dopant. This clearly shows that the dopants that are used by Sachitano are not substantially identical. Because the dopants that are used by Sachitano are not substantially identical they also do not have substantially identical dopant concentrations.

Sachitano later implants the base region 150 of the NPN transistor. "Masking and boron implant steps (steps 37 and 38) provide P-type base region 150 for the bipolar transistor in region 114 and lightly-doped P-source and drain regions 152, 154 for the PMOSFET in region 118." (Sachitano, Column 8, Lines 45-49). Sachitano described a single implant step for the base of the NPN transistor and the lightly doped source/drain regions of the PMOS transistor. However, this implantation does not affect the shielded gate regions of the MOS transistors.

For the reasons set forth above, the Applicants respectfully submit that the Sachitano reference does not teach or suggest that "a base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopant concentrations." The Applicants respectfully submit that this feature is not inherent in the Sachitano reference.

Accordingly, the Applicants respectfully traverse all of the anticipation rejections of Claims 1-3, 7-9, 13-17 and 21 and respectfully requests the Examiner to withdraw the § 102 rejections with respect to these claims.

II. CLAIM REJECTIONS -- 35 U.S.C. § 103

1. Claims 1-3, 7-9, 13-17 and 21 were rejected under 35 U.S.C. § 103(a) as being obvious over Sachitano in view of U.S. Patent No. 5,028,557 to Tsai et al. (hereinafter "Tsai").

2. Claims 4, 10 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sachitano in view of U.S. Patent No. 6,441,441 to Kakutaro Suda (hereinafter "Suda").

3. Claims 4, 10 and 20 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Sachitano in view of Tsai in view of Suda.

In response, the Applicants have amended Claim 1. The Applicants respectfully traverse these rejections. The Applicants reiterate and incorporate by reference all of the comments and arguments previously made with respect to the Sachitano reference.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 4, October 2005). Absent such a prima facie case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.* Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

The September 25, 2007 Office Action suggested that is would have been obvious in view of the Tsai reference to use phosphorus as an N-type dopant in the base of the PNP transistor of Sachitano. (September 25, 2007 Office Action, Page 4, Lines 15-17). The Applicants respectfully traverse this assertion. The Applicants also respectfully traverse the assertion that the Sachitano reference teaches that the base of a double poly bipolar transistor (140) and a gate of a double poly MOS transistor (148) contain substantially identical dopants. For the reasons previously set forth and described, the Sachitano reference uses different dopants. Because the dopants that are used by Sachitano are not substantially identical they also do not have substantially identical dopant concentrations.

Even if the Tsai reference and the Sachitano reference could be properly combined (which the Applicants do not admit) the combination would still not teach, suggest or even hint at the Applicants' invention as claimed in amended Claim 1 and its dependent claims.

Accordingly, the Applicants respectfully request the Examiner to withdraw the § 103 rejections with respect to Claims 1-3, 7-9, 13-17 and 21.

Because Claims 4, 10 and 20 are dependent claims, Claims 4, 10 and 20 each require that "at least one double poly bipolar transistor is an NPN transistor and wherein said at least one double poly MOS transistor is a PMOS transistor," where the base of the double poly bipolar transistor and a gate of the double poly metal oxide semiconductor transistor contain substantially identical dopant concentrations. Neither Sachitano nor Suda nor Tsai teaches or suggests this feature. The Applicants respectfully submit that the neither the Suda reference nor the Tsai reference remedies the deficiencies of the Sachitano reference.

Suda describes, variously, a PMOS transistor and an NPN bipolar transistor, and indicates in each case that boron is acceptable as a P-type dopant. Suda does not explicitly teach that these two structures contain substantially identical dopant concentrations, and certainly one could be heavily doped while the other is lightly doped.

The Examiner suggested that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the P-type transistor gate of the PMOS device of Suda in the BiCMOS process of Sachitano, or Sachitano in view of Tsai. One would have been motivated to do this because Suda taught that P-type gates and N-type gates were art recognized functional equivalents for forming the conductive gate of a PMOS transistor (col. 9, lines 57-65) (MPEP § 2144.06)." (September 25, 2007 Office Action, Page 6, Lines 19-24).

The Applicants respectfully traverse this assertion of the Examiner. Even if the Suda reference (or the Tsai reference) could be properly combine with the Sachitano reference (which the Applicants do not admit) the combination would still not teach, suggest or even hint at the Applicants' invention as claimed in amended Claim 1 and its dependent claims.

Nothing in the prior art of reference, nor in the knowledge generally available to those of skill in the art at the time of the invention, would motivate one to make the specific combination and modification necessary to produce the claimed invention.

The Applicants respectfully submit that one of ordinary skill, having only Sachitano before him, would not be prospectively moved to spontaneously assume that the substantial disclosure of Sachitano was in need of a base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopant

concentrations. In fact, the Applicants respectfully submit that Sachitano appears to suggest differentiated doping during formation. (Column 4, Line 55 to Column, Line 7; Column 10, Lines 31-51).

In order to overcome the admitted deficiencies of Sachitano, the Examiner selectively culls from Suda the inference of a base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor containing substantially identical dopants – even though Suda itself does not explicitly teach that these two structures contain substantially identical dopants. The Examiner further ignores the fact that, in order to combine the references as suggested, one of ordinary skill in the art would have to completely overlook the remainder of Suda's various teachings of PMOS transistor and an NPN bipolar transistor structure and formation – teachings that vary significantly from Sachitano's.

The Examiner offers that "P-type gates and N-type gates were art recognized functional equivalents for forming the conductive gate of a PMOS transistor" (September 25, 2007 Office Action, Page 6, Lines 22-24) as the motivation for one of ordinary skill in the art to embark on this speculative and selective combination process. This has no bearing at all on the Applicants' use of substantially identical dopant concentrations, as claimed.

In summary, there is neither a motivation nor a suggestion in either the cited references or the knowledge of a person of ordinary skill in the art at the time of the Applicant's invention to: 1) spontaneously assume a deficiency in Sachitano; 2) seek out and find Suda; 3) ignore almost all of Suda's teachings of structure and process; 4) selectively cull a single concept from Suda – a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor transistor

containing substantially identical dopants – even though Suda does not explicitly disclose such; and 5) substantially modify the processes and structures of Sachitano to incorporate this spontaneous extraction of concept from Suda. Furthermore, even if the references were to be so selectively combined, the combination would still not result in the Applicant's invention as recited in amended Claim 1 or dependent Claims 4, 10 and 20 of the patent application.

Accordingly, the Applicants respectfully request the Examiner to withdraw the § 103 rejections with respect to Claims 4, 10 and 20.

All claim rejections are respectfully traversed. Reconsideration and allowance of the pending claims (Claims 1-4, 7-10, 13-17 and 20-21) are respectfully requested.

III. ADDITIONAL COMMENTS

In the Sachitano reference, both the PMOS device and NMOS device are doped with an N type dopant (phosphorus). The Sachitano reference also uses a separate mask and a P type implant (boron) for the NPN extrinsic base. While in the case of providing only an NPN device, this mask count is mask count neutral when compared to the mask count of the Applicants' invention. This is because the Sachitano reference uses a single mask for the PMOS and NMOS active regions. However, in making complementary BiCMOS the Sachitano method would require an additional mask for the PNP extrinsic base. In contrast, in making complementary BiCMOS the Applicants' invention would save one mask and implant procedure.

The Sachitano method also adds a separate intrinsic base implant. This is because it includes the PMOS PLDD in the NPN intrinsic base but adds an additional dedicated mask and

implant to augment the base doping. In contrast, the Applicants' invention uses the same mask and implant to form the PLDD and the NPN intrinsic base and the NLDD and the PNP intrinsic base. In the case of complementary bipolar or complementary BiCMOS, this feature saves two masking layers and implants (and the associated cycle time and costs) over the prior art.

The complementary doping of the MOS gates in the Applicants' invention enables complementary doping of the extrinsic base and, therefore, the formation of both NPN devices and PNP devices. The complementary doping of the gates provides better threshold matching and control. For these reasons, the Applicants' invention provides significant improvements over the technology that is disclosed in the prior art.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting prosecution of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckbutrus.com*.

No fees are believed to be necessary. However, in the event that any fees are required for the prosecution of this application (including extension of time fees), the Commissioner is hereby authorized to charge any necessary fees to Deposit Account No. 50-0208.

Respectfully submitted,

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